UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,923	10/17/2003	Tommy Lai	1016-024	4860

22898 7590 12/13/2005

THE LAW OFFICES OF MIKIO ISHIMARU
333 W. EL CAMINO REAL
SUITE 330
SUNNYVALE, CA 94087

EXAMINER	
TOLEDO, FERNANDO L	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/689,923	LAI ET AL.	
	Examiner	Art Unit	
	Fernando L. Toledo	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 5-20* is/are pending in the application.

4a) Of the above claim(s) *11-20* is/are withdrawn from consideration.

5)☒ Claim(s) *7-10* is/are allowed.

6)☒ Claim(s) *1,2,5 and 6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of claims 1 – 10 in the reply filed on 30 March 2005 is acknowledged. The traversal is on the ground(s) that it "is now established common practice for Examiners in the United States Patent and Trademark Office ("USPTO") regularly and without objection to perform searches -in a single application- on related method and device claims in applications filed in the USPTO under the Patent Cooperation Treaty ("PCT"). This practice is in conformance with the requirements of PCT Rule 13, and because the USPTO is a PCT receiving office, the USPTO is bound by the PCT rules." This is not found persuasive because the application is not the National Stage of an international application or PCT or was not filed according to the rules of 35 USC 371. Hence, a restriction is allowed according to 35 USC 121. See MPEP §806.05(f).

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 1 – 5 are rejected under 35 U.S.C. 102(a) as being anticipated by Watt (U. S. Patent 6,586,296 B1).

In re claim 1, Watt, in the U. S. Patent 6,586,296 B1; figures 1 – 19 and related text, discloses forming at least on oxide-nitride-oxide dielectric layer 124 above the semiconductor substrate 100; and forming at least one well 122 and threshold implantation 134 into at least one of an array area and a periphery area of the semiconductor substrate beneath the oxide-nitride-oxide dielectric layer subsequent to the formation of the oxide-nitride-oxide layer; and forming at least one other well 114 and threshold implantation 118 into the other of the array and periphery areas of the semiconductor substrate.

4. In re claim 2, Watt discloses at least one channel implantation into at least one area of the semiconductor substrate beneath the oxide-nitride-oxide dielectric layer subsequent to the formation of the oxide-nitride-oxide dielectric layer (Figures 11a and 11b).

5. In re claim 5, Watt discloses further including forming a channel implantation into the array area and the periphery area (Figures 12 and 13).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (US Patent Application Publication US 2003/00232472 A1) in view of Watt.

Wu, in the US Patent Application Publication US 2003/00232472 A1; figures 1A – 7C and related text, discloses providing a semiconductor substrate 300; forming an nitraded oxide

dielectric layer 301 on the semiconductor substrate; forming a layer of polysilicon 303 on the nitraded oxide dielectric layer; forming a nitride hardmask layer 303 ion the layer of polysilicon; patterning and forming a composite mask PR1 on the nitride hardmask; etching the nitride hardmask, layer of polysilicon, nitrided oxide dielectric layer, and semiconductor substrate to form shallow trench isolation trenches (Figure 3B); filling the shallow trench isolation trenches with an oxide gap fill (Figure 3B); polishing the oxide gap fill (Figure 3C); and removing the nitride hardmask (Figure 3D).

Wu does not teach forming an oxide-nitride-oxide dielectric layer. Also, Wu does not teach covering a periphery area over the semiconductor substrate with a photoresist mask; and performing well and threshold implantation over an array area above the semiconductor substrate into the semiconductor substrate beneath the oxide-nitride-oxide dielectric layer. However, Watt discloses that a dielectric layer can be formed by a nitraded oxide or an oxide-nitride-oxide (Column 5, Lines 5 – 14). Furthermore, Watt discloses covering a periphery area over the semiconductor substrate with a photoresist mask128; and performing well and threshold implantation over an array area above the semiconductor substrate into the semiconductor substrate beneath the oxide-nitride-oxide dielectric layer (Figure 10) to form wells and channel thresholds to enable NMOS and PMOS transistors to be formed on the same substrate (Column 1, Lines 25 – 31 and 38 – 43).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a oxide-nitride-oxide layer in the invention of Wu, instead of a nitraded oxide layer, since as taught by Watt, an oxide-nitride-oxide as well as a nitraded oxide can be used as a dielectric layer.

Also, it would have been obvious to one of ordinary skill in the art at the time the invention was made to cover a periphery area over the semiconductor substrate with a photoresist mask; and perform a well and threshold implantation over an array area above the semiconductor substrate into the semiconductor substrate beneath the oxide-nitride-oxide dielectric layer in the invention of Wu, since as taught by Watt, it will form wells and channel thresholds to enable NMOS and PMOS transistors to be formed on the same substrate.

Allowable Subject Matter

8. Claims 7 –10 are allowed over the prior art of record.

Response to Arguments

9. Applicant's arguments filed 14 September 2005 have been fully considered but they are not persuasive for the following reasons.

10. Applicant contests that Watt does not teach threshold adjustment in the periphery or array area. Examiner respectfully submits that Watt teaches a channel implantation after a well implantation, in both, the periphery and array area, that channel implantation is the threshold voltage implantation.

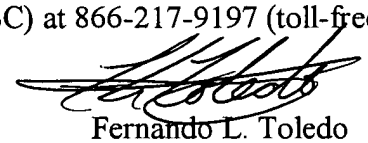
11. Applicant's arguments with respect to claim 6 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fernando L. Toledo whose telephone number is 571-272-1867. The examiner can normally be reached on Mon-Thu 7am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Fernando L. Toledo
Patent Examiner
Art Unit 2823

flt
7 December 2005